FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR
KIX0136-PCT	09/763573

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP99/04624	26 AUGUST 1999	31 AUGUST 1998

TITLE OF INVENTION
SEMICONDUCTOR DEVICE AND SUBSTRATE FOR MOUNTING THE SAME

APPLICANT(S) FOR DO/EO/US
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Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☒ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
9. ☒ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☐ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

ACKNOWLEDGEMENT POSTCARD

528 Rec'd PCT/PTO 26 FEB 2001

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR) 09776573	INTERNATIONAL APPLICATION NO. PCT/JP99/04624	ATTORNEY'S DOCKET NUMBER KIX0136-PCT

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	$1,000.00	
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	$860.00	
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	$710.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$690.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	$100.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =		$860.00
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).		$0.00

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	10 - 20 =	0	x $18.00	$0.00
Independent claims	2 - 3 =	0	x $80.00	$0.00
Multiple Dependent Claims **(check if applicable).**			☐	$0.00

TOTAL OF ABOVE CALCULATIONS =		$860.00
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable).**	☐	$0.00
SUBTOTAL =		$860.00
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +		$0.00
TOTAL NATIONAL FEE =		$860.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**	☒	$40.00
TOTAL FEES ENCLOSED =		$900.00
	Amount to be: refunded	$
	charged	$

☒ A check in the amount of **$900.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **50-1390** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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32,329
REGISTRATION NUMBER

FEBRUARY 26, 2001
DATE

SPECIFICATION

SEMICONDUCTOR DEVICE AND SUBSTRATE FOR MOUNTING THE SAME

Technical Field

The present invention relates to a semiconductor device, and more specifically to a semiconductor device having a light emitting capability and/or a light receiving capability. Further, the present invention relates to a circuit substrate for supporting such a semiconductor device as the above. Still further, the present invention relates to a combination of the semiconductor device and a storage receptacle for collectively holding a plurality of the semiconductor devices.

Background Art

Fig. 20 and Fig. 21 show a prior art semiconductor device. This semiconductor device X is a light emitting diode (LED), and includes a first lead 100, a second lead 200, a semiconductor chip 300 as a light emitting element, a connecting wire W, and a protective package 400.

The semiconductor chip 300 is placed at an inner end 100a of the first lead 100. The semiconductor chip 300 has an upper surface 330 electrically

connected with an inner end 200a of the second lead 200 via a wire W. The protective package 400 is made of a transparent resin such as an epoxy resin, and completely covers the semiconductor chip 300 and the connecting wire W. Further, the protective package 400 partially covers the first and the second leads 100, 200. In Figs. 20 and 21, the inner portion of the first lead 100 covered by the protective package 400 is indicated by numeral code 110 whereas the outer portion of the first lead 100 extending out of the protective package 400 is indicated by numeral code 111. Like the first lead 100, the second lead 200 also has an inner portion 220 covered by the protective package 400 and an outer portion 221 extending out of the protective package 400.

As shown in Fig. 21, the inner portion 110 of the first lead 100 extends straightly whereas the outer portion 111 is bent. The outer portion 111 of the first lead 100 has a free end 111a flush with a bottom surface of the protective package 400. The second lead also has the same constitution as the first lead, and thus has a free end 221a flush with the bottom surface of the protective package 400.

The circuit substrate 5 is provided with pads 52a, 52b for establishing electrical connection with the semiconductor device X. The semiconductor device X is mounted on the circuit substrate 5, with the free

ends 111a, 221a connected with the pads 52a 52b respectively.

The prior art semiconductor device X is inconvenient in the following points: Specifically, the semiconductor device X is mounted on the circuit substrate 5 via the leads 100, 200 which are bent as described above. In such a case, as shown in Fig. 21, the entire protective package 400 of the semiconductor device X comes above the circuit substrate 5. This leads to a problem that a dimension Dh between a top Ap of the semiconductor device X and an upper surface of the circuit substrate 5 becomes large.

DISCLOSURE OF THE INVENTION

It is therefore an object of the present invention to provide a semiconductor device capable of solving or at least reduce the problem described above.

Another object of the present invention is to provide a circuit substrate for mounting such a semiconductor device as the above.

Still another object of the present invention is to provide a combination of a plurality of the semiconductor devices and a storage receptacle for collectively holding these semiconductor devices.

According to a first aspect of the present invention, there is provided a semiconductor device

comprising: a semiconductor chip; a protective package covering the semiconductor chip; a first lead conducting to the semiconductor chip, including an inner portion covered by the protective package and at least one outer portion extending out of the protective package; a second lead conducting to the semiconductor chip, including an inner portion covered by the protective package and at least one outer portion extending out of the protective package; wherein each of the outer portions of the first lead and the second lead is flat.

Preferably, the outer portion of the first lead and the outer portion of the second lead extend in a same plane.

Further, the inner portion and the outer portion of the first lead, and the inner portion and the outer portion of the second lead may extend in a same plane.

According to a preferred embodiment of the present invention, each of the first lead and the second lead has a plurality of outer portions extending out of the protective package, and the outer portions extend in a same plane.

Preferably, the protective package includes at least a pair of opposed side surfaces, and each of the side surfaces has a first slanted portion and a second slanted portion.

The first slanted portion and the second slanted portion may be flat and meet with each other at a predetermined angle.

The semiconductor chip is a light emitting element for example. Also, the semiconductor chip is a light receiving element for example.

According to another preferred embodiment of the present invention, the semiconductor device further comprises an additional semiconductor chip, a third lead conducting to the additional semiconductor chip, and a fourth lead conducting to the additional semiconductor chip. The third lead includes an inner portion covered by the protective package and a flat outer portion extending out of the protective package, and the fourth lead includes an inner portion covered by the protective package and a flat outer portion extending out of the protective package.

According to a second aspect of the present invention, there is provided a circuit substrate for mounting a semiconductor device including a protective package and flat leads extending out of the protective package. The substrate comprises: a main surface formed with a predetermined wiring pattern; a plurality of connecting pads formed in the main surface for conduction to the leads of the

semiconductor device; and a through hole corresponding to a shape of the protective package.

Preferably, the connecting pads are disposed around the through hole.

Preferably, the main surface mounted with the semiconductor device is laminated with a coating member.

According to a third aspect of the present invention, a combination of a plurality of semiconductor devices and a storage receptacle for storing the same is provided: each of these semiconductor devices includes an upper surface having a predetermined function, and a bottom surface away from the upper surface, whereas the storage receptacle includes a carrier member having a plurality of recesses opening upward, and a covering tape having an adhesive surface attached to the carrier member, and the semiconductor device is housed in the recess with the bottom surface facing upward.

According to a preferred embodiment of the present invention, the upper surface of the semiconductor device is formed with a light-condensing portion.

Preferably, each of the recesses includes a larger space and a smaller space.

Preferably, the recesses are formed longitudinally of the carrier member at a predetermined interval.

Other objects, characteristics, and advantages of the present invention will become clearer from the following description of embodiments to be presented with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a perspective view of a semiconductor device as a first embodiment of the present invention.

Fig. 2 is a sectional view taken in lines I-I in Fig. 1.

Fig. 3 is a perspective view of a semiconductor device as a second embodiment of the present invention.

Fig. 4 is a sectional view taken in lines II-II in Fig. 3.

Fig. 5 is a plan view of the semiconductor device in Fig. 3.

Fig. 6 is a plan view of a lead frame used for manufacture of the semiconductor device according to the present invention.

Fig. 7 is a diagram for describing a wire-bonding step.

Fig. 8 is a sectional view showing a packaging step.

Fig. 9 is a diagram for describing a step in which the semiconductor device according to the present invention is mounted on a circuit substrate.

Fig. 10 a sectional view showing a use of the semiconductor device according to the present invention.

Fig. 11 a perspective view of a semiconductor device as a third embodiment of the present invention.

Fig. 12 a plan view of the semiconductor device in Fig. 11.

Fig. 13 is a diagram showing constituent elements of the semiconductor device.

Figs. 14~17 are diagrams for describing manufacturing steps of the semiconductor device in Fig. 11.

Fig. 18 is a sectional view of a storage receptacle for collectively holding a plurality of the semiconductor devices.

Fig. 19 is a diagram showing a state in which the semiconductor device is being taken out of the storage receptacle in Fig. 18.

Fig. 20 is a perspective view of a prior art semiconductor device.

Fig. 21 is a sectional view taken in lines III - III in Fig. 20.

BEST MODE FOR CARRYING OUT THE INVENTION

Now, preferred embodiments of the present invention will be described with reference to the accompanying drawings, Fig. 1~19.

First, reference is made to Figs. 1 and 2. These figures show a semiconductor device according to a first embodiment of the present invention. This semiconductor device A according to the present embodiment has a light emitting capability as will be described later. However, the present invention is not limited to this embodiment, and can be applicable to other semiconductor devices.

As shown in Figs. 1 and 2, the semiconductor device A comprises a first lead 1, a second lead 2 spaced from the first lead 1, and a semiconductor chip 3 having a light emitting capability. The semiconductor chip 3 is supported on an end 10a of the first lead 1, and has an upper surface 30 electrically connected with an end 20a of the second lead 2 via a wire W.

The semiconductor device A further comprises a protective package 4 made of a transparent resin. The protective package 4 includes a main body portion 40 which is generally rectangular parallelepiped, and

a light condensing portion 44 formed on an upper surface of the main body portion. The light condensing portion 44 is provided so as to prevent diffusion of light emitted by the semiconductor chip 3.

The protective package 4 entirely covers the semiconductor chip 3 and the wire W, and partially covers the first lead 1 and the second lead 2. With this constitution, the first lead 1 includes an inner portion 10 covered by the protective package 4 and an outer portion 11 extending out of a first side surface 42 of the protective package 4. Likewise, the second lead 2 also includes an inner portion 20 covered by the protective package 4 and an outer portion 21 extending out of the second side surface 43 of the protective package 4.

As shown in Figs. 1 and 2, the first lead 1 and the second lead 2 are flat as a whole. Therefore, the outer portions 11, 21 of the first lead 1 and the second lead 2 are also flat. As clearly shown in Fig. 2, in a vertical relationship (i.e. directions indicated by reference code Vd), the first lead 1 and the second lead 2 are located at a center of the main body portion 40 of the protective package 4. Further, the first lead 1 and the second lead 2 extend in parallel to a bottom surface 41 of the protective package 4. Therefore, the outer portion 11 of the

first lead 1 is vertical to the first side surface 42 of the protective package 4 whereas the outer portion 21 of the second lead 2 is vertical to the second side surface 43 of the protective package 4.

The semiconductor device A with the constitution described above is mounted on the circuit substrate 5 as shown in Fig. 2. Specifically, the circuit substrate 5 has a main surface 51 (a lower surface in Fig. 2) provided with connecting pads 52 at locations corresponding to the outer portion of the first lead 1 and the outer portion 21 of the second lead 2. Though not illustrated, the main surface 51 is formed with a predetermined wiring pattern connecting with these connecting pads 52. Further, the circuit substrate 5 is provided with a through hole 50 between the connecting pads 52 for fitting the semiconductor device A.

The semiconductor device A is fitted into the through hole 50, with the light condensing portion 44 facing away from the main surface 51 of the circuit substrate 5. The outer portion 11 and 21 of the first lead 1 and the second lead 2 are connected to respective connecting pads 52 via solder 53. According to the mounting method described as above, the distance Dh between the top of the light condensing portion 44 and a second surface 51a of the substrate 5 can be made smaller than in the prior art.

Reference is now made to Figs. 3~5. These figures show a semiconductor device B according to a second embodiment of the present invention. It should be noted here that components substantially the same as in the first embodiment are indicated by the same reference codes in Figs. 3~5.

As shown in Fig. 3, the semiconductor device B has a first lead 1' to which the semiconductor chip 3 is bonded, and the second lead 2'. The semiconductor chip 3 is connected to the second lead 2' via a wire W. The semiconductor device B further has a protective package 4' for protecting the semiconductor chip 3 and the wire W. The protective package 4' has an opposed pair of side surfaces 42' and 43' (hereinafter called the first side surface 42' and the second side surface 43'), out of which the first lead 1' and the second lead 2' extend respectively. The protective package 41 has another opposed pair of side surfaces 45' and 46'. The protective package 4' further has a light condensing portion 44' for appropriately condensing light emitted by the semiconductor chip 3.

As shown in Fig. 4, each of the first side surface 42' and the second side surface 43' of the protective package 4' includes two slanted surfaces. Specifically, the first side surface 42' includes an upper slanted surface slanted at an angle of α with

respect to the vertical line, and a lower slanted surface slanted at an angle of β to the same vertical line. Likewise, the second side surface 43' and other side surfaces 45', 46' include an upper slanted surface and a lower slanted surface respectively. The angles α and β may be 5~10 degrees for example. The angles α and β may be the same or may be different from each other.

As shown in Fig. 5, the first lead 1' includes an inner portion 10' covered by the protective package 4' and a first outer portion 11' and a second outer portion 12' each extending out of the protective package 4'. The inner portion 10' and the two outer portions 11', 12' extend in a plane parallel to a bottom surface 41' of the protective package 4'. Further, the first lead 1' has a supporting pad 10'a to be mounted with a semiconductor chip 3. The supporting pads 10'a is located between the first lead 1' and the second lead 2', being connected to the inner portion 10' of the first lead 1' via a connecting portion 10'b.

The second lead 2' includes an inner portion 20' covered by the protective package 4' and a first outer portion 21' and a second outer portion 22' each extending out of the protective package 4'. As in the first lead 1', the inner portion 10' and the two outer portions 21', 22' of the second lead 2' also

extend in the plane parallel to the bottom surface 41' of the protective package 4'.

The semiconductor device B with the constitution described above is fitted into a through hole 50 formed in the circuit substrate 5 as is the semiconductor device A according to the first embodiment, and then fixed to the circuit substrate 5 via solder 53.

As has been described, each of the side surfaces 42', 43', 44', 45' of the semiconductor device B according to the second embodiment includes the upper slanted surface and the lower slanted surface (See Fig. 4.) Therefore, the semiconductor device B can be easily inserted into the through hole 50 of the circuit substrate 5. By adjusting the angle α, the size of the protective package 4', and the size of the through hole 50, it becomes possible to make easy the insertion of the protective package 4' into the through hole 50, and to reliably fit the protective package 4' into the through hole 50.

As shown in Fig. 3, the side surface 46' of the protective package 4' is formed with a cutout 46'a. The cutout 46'a is an indication of the polarity of semiconductor device B. For example, one of the two leads 1', 2' which is closer to the cutout 46' (i.e. the second lead 2' according to Fig. 3) may be predetermined to be negative. With such an

arrangement as the above, the semiconductor device B can be appropriately inserted to the through hole 50 of the circuit substrate 5.

In the semiconductor device B according to the second embodiment, each of the first lead 1' and the second lead 2' has two outer portions. Therefore, the circuit substrate 5 needs a total of four connecting pads 52. However, as will be understood from Fig. 5, if the outer portion 11' of the first lead 1' is conductive to the corresponding connecting pads 52, the other outer portion 12' does not need to be conductive to its corresponding connecting pads 52. Specifically, the outer portion 12' may only be fixed mechanically to its corresponding pad 52. The same applies to the outer portions 21', 22' of the second lead 2'. By attaching the semiconductor device B to the circuit substrate 5 via the four outer portions 11', 12', 21', 22' as described above, the semiconductor device B can be mounted stably on the circuit substrate 5.

Next, a method for manufacturing the semiconductor device B having the above constitution will be described with reference to Figs. 6~8.

Fig. 6 is a plan view showing a lead frame used for the manufacture of the semiconductor device B. The lead frame 6 shown in the figure can be obtained by punching out a metal plate made of cupper, iron

and so on. The lead frame 6 includes a pair of side bars 60 extending in parallel to each other. Further, the lead frame 6 has a plurality of cross member pairs 61 interconnecting the side bars 60. The cross bar pairs 61 are disposed at an interval longitudinally of the side bars 60. Each of the cross bar pairs 61 includes a first cross bar 61a and a second cross bar 61b extending vertically with respect to the longitudinal direction of the side bar 61. The first cross bar 61a has a center portion formed with a bonding pad 10'a.

A semiconductor chip 3 is bonded to each of the bonding pads 10'. If the semiconductor device B is constituted as a light emitting device, the semiconductor chip 3 is provided by a light emitting diode for example. If the semiconductor device B is constituted as a light receiving device, the semiconductor chip 3 is provided by a phototransistor for example. Of course, other semiconductor chips may be used.

Next, as shown in Fig. 7, an upper surface 30 of the semiconductor chip 3 and the second cross bar 61b are connected by a wire W. The connection of the wire W can be made by using a bonding tool 7. Specifically, a tip portion of the wire W is extended out of a lower end portion of the bonding tool 7. Then, the tip portion is melted into a ball of molten. Then, the

bonding tool 7 is moved downward, pressing the molten ball onto the upper surface of the semiconductor chip 3 (first bonding). Thereafter, while pulling the wire W out of the lower end portion of the bonding tool 7, the bonding tool is moved to the location of the second cross bar 61b. Finally, the wire W is press-fitted to the second cross bar 61b (second bonding). In order to perform the wire bonding appropriately, the lead frame 6 should preferably be heated by a heater (not illustrated) incorporated in a supporting table 8. Alternatively, the bonding tool 7 may be supplied with ultrasonic wave when performing the second bonding.

Next, by using a predetermined molding apparatus, a protective package 4' is formed in a region P enclosed by phantom lines (Fig. 6) of the lead frame 6. Each of the protective package 4' is formed as follows:

First, as shown in Fig. 8, the semiconductor chip 3 is housed in a cavity 90 formed by an upper mold member 9A and a lower mold member 9B. Next, under this particular state, a molten thermosetting resin (an epoxy resin for example) is injected into the cavity 90. Finally, after the injected resin has been set, the upper mold member 9a and the lower mold member 9B are moved upward and downward respectively, to take out the solid resin, i.e. the protective

package 4'. By this molding operation, the light condensing portion 44' is formed simultaneously.

As shown in Fig. 8, the upper mold member 9A has downwardly widening inner side surfaces 9Aa whereas the lower mold member 9B has upwardly widening inner side surfaces 9Ba. For this reason, when the resin set in the cavity 90 is taken out, the solid body of resin can be easily separated from the upper mold member 9A and the lower mold member 9B.

If the semiconductor device B is constituted as the light emitting device or a light receiving device, the protective package 4' is formed of a highly transparent resin (for example an epoxy resin). Otherwise, the protective package 4' may not necessarily be formed of a highly transparent resin, or it is not necessary to provide the light condensing portion 44' depending on the application.

The semiconductor device B can be constituted so as to selectively receive an infrared ray. In this case, the protective package 4' may be of a transparent material, but is preferably formed of a black resin in order to effectively prevent the reception of rays other than the infrared ray.

After the protective package 4' is formed, the first and the second cross bars 61a, 61b are cut at predetermined locations (indicated by dashed lines in Fig. 6) to obtain a finished semiconductor device

B (Fig. 3). The semiconductor device B thus obtained may be mounted on the circuit substrate 5 with another semiconductor device for light reception, a photo sensor can be manufactured.

Fig. 9 shows a step of mounting the semiconductor device B according to the second embodiment of the present invention on the circuit substrate 5. (The circuit substrate 5 shown in the figure has a light receiving semiconductor device B' already mounted.) As shown in this particular figure, the circuit substrate 5 is formed with a through hole 50e for fitting the semiconductor device B. The through hole 50e is spaced from another through hole 50r for the light receiving semiconductor device B' by a predetermined distance.

The circuit substrate 5 has a main surface 51 provided with four connecting pads 52 near the through hole 50e. These pads 52 are to be connected with the outer portions 11', 12' of the first lead 1', and the outer portions 21', 22' of the second lead 2' of the semiconductor device B.

When the semiconductor device B is fitted into the through hole 50e, a suction collet K as shown in Fig. 9 may be used. In this case, a bottom surface 41' of the semiconductor device B is sucked by the suction collet K, and then the collet K is moved toward the circuit substrate 5 to insert the semiconductor

device B into the through hole 50e. (See indication by dashed lines in Fig. 9.)

After the semiconductor device B is appropriately fitted into the through hole 50e, the circuit substrate 5 mounted with the semiconductor device B (and the semiconductor device B') undergoes a heat treatment. Though not illustrated in the figure, each of the connecting pads 52 is applied with solder paste in advance. Therefore, by heat-treating the circuit substrate 5, the applied solder becomes molten, and by cooling the circuit substrate 5 thereafter, the outer portions 11', 12', 21' 22' of the first lead 1' and the second lead 2' are fixed to respective connecting pads 52.

After mounting the semiconductor devices B and B' on the circuit substrate 5, as shown in fig. 10, a coating member 53 is applied on the main surface 51 of the circuit substrate 5. As a result, the semiconductor devices B, B' are coated by the coating member 54. Through such a process as described above, a unit C including the semiconductor devices B, B' and the circuit substrate 5 is obtained. The coating member 54 is preferably provided by an electrically insulating and optically nontransparent resin for example. By using the coating member 54 provided by such a resin material, light, electrical noise and so on from outside of the unit C can be shielded.

As shown in Fig. 10, the unit C can be used in a CD player for detecting presence of a disc D. Specifically, the unit C is disposed in the CD player, so that the light condensing portions 44' of the semiconductor devices B, B' face the inserted disc D. If the disc D is absent, light emitted from the semiconductor device B advances a path indicated by dashed lines in Fig. 10, and reaches the semiconductor device B'. (The member P disposed across the path is a prism.) On the other hand, if the disc D is inserted in the CD player, the path described above is blocked by the disc D, and the light emitted from the semiconductor device B is not received by the semiconductor device B'.

The above described unit C utilizing the semiconductor devices B, B' according to the present invention, can be made more compactly than a unit utilizing prior art semiconductor devices and the substrate. (See Fig. 21.) Therefore, as shown in Fig. 10, the disc D can be placed closer to the second surface 51a of the circuit substrate 5 than in the prior art. As a result, it becomes possible to decrease a detecting space for the photo sensor incorporated in the CD player.

Next, a semiconductor device according to a third embodiment of the present invention will be described with reference to Figs. 11~13. As will be understood

from Fig. 13, the semiconductor device according to the third embodiment is a photo sensor in which a light emitting semiconductor element is packaged together with a light receiving semiconductor element.

Specifically, the illustrated semiconductor device E, comprises a light emitting semiconductor chip 3, a light receiving semiconductor chip 3', and a protective package 4' covering these semiconductor chips. Further, the semiconductor device E has a generally flat first lead 1 and a second lead 2 each conducting to the semiconductor chip 3, and further has a generally flat first lead 1' and a second lead 2' each conducting to the semiconductor chip 3'. Each of the first leads 1, 1' and the second leads 2, 2' partially extends out of the protective package 4'. The protective package 4' according to the third embodiment has an outlook generally the same as the one shown in Fig. 3, differing however, in that no light condensing portion is provided, and that a cutout 46' is formed at a corner portion of the protective package 4'.

The protective package 4' has a first transparent resin portion 4'a incorporating the semiconductor chip 3, a second transparent resin portion 4'b incorporating the light receiving semiconductor chip 3', and a third, non-transparent resin portion

4'c holding the resin portions 4'a, 4'b. The first and the second resin portions 4'a, 4'b have respective upper surfaces and bottom surfaces not covered by the third resin portion 4'c and therefore exposed to outside. The first and the second resin portions 4'a, 4'b are formed of a transparent epoxy resin for example whereas the third resin portion 4'c is formed of a black resin for example.

In a side view, the semiconductor chip 3 is placed generally at a vertically central location in the first resin portion 4'a, on an inner portion 10 of the first lead 1 whereas the semiconductor chip 3' is placed at a generally central location in the second resin portion 4'b, on an inner portion 10' of the other first lead 1'. The upper surfaces of the semiconductor chips 3, 3'are electrically connected with inner portions 20, 20' of the second leads 2, 2' respectively via wires W.

As shown in Fig. 13, the semiconductor chip 3 can be provided by an LED whereas the semiconductor chip 3' can be provided by a phototransistor. Alternatively to the phototransistor, a photo diode may be used.

The semiconductor device E having the constitution described as above can be manufactured in the following steps to be described below.

First, a lead frame 6' as shown in Fig. 14 is prepared by punching out a thin metal plate for example. The lead frame 6' includes a first and a second side bars 60'a, 60'b, extending in parallel to each other, and a plurality of cross bars 63' (Fig. 14 shows only two cross bars). The cross bars 63' are spaced from the adjacent ones by a predetermined interval T longitudinally of the lead side bars 60'a, 60'b.

In a region between a pair of mutually adjacent cross bars 63', a pair of lead portions 62'c, 62'd and another pair of lead portions 64'c, 64'd are disposed. The lead portions 62'c, 64'c extend from the first side bar 60'a toward the second side bar 60'b. On the other hand, the lead portions 62'd, 64'd extend from the second side bar 60'b toward the first side bar 60'a. The lead portions 62'c, 64'c have free ends formed with chip bonding portions 62'a, 64'a respectively. Further, the lead portions 62'd, 64'd have free ends formed with wire bonding portions 62'b, 64'b respectively.

The lead frame 6' having the constitution as described above is mounted with a light emitting semiconductor chip 3 and the light receiving semiconductor chip 3'. Specifically, as shown in Fig. 15, the light emitting semiconductor chip 3 is bonded to the chip bonding portion 62'a whereas the

light receiving semiconductor chip 3' is bonded to the chip bonding portion 64'a. Thereafter, the upper surface of the semiconductor chip 3 and the wire bonding portion 62'b are electrically connected by the wire W whereas the upper surface of the semiconductor chip 3' and a wire bonding portion 64'b are electrically connected by a wire W'.

Next, as shown in Fig. 16, the semiconductor chip 3 and the wire W are molded and thereby covered by a transparent resin body 47a (hereinafter called the first resin body), and the semiconductor chip 3' and the wire W' are molded and thereby covered by another transparent resin body 4'b (hereinafter called the second resin body)(The first molding step).

Next, as shown in Fig. 17, the first and the second resin bodies 4'a, 47b are covered by a non-transparent resin body (hereinafter called the third resin body) (The second molding step). In this step, the upper surfaces and the bottom surfaces of the first and the second resin bodies 4'a, 4'b are left exposed to outside.

Finally, the four lead portions 62'c, 62'd, 64'c, 64'd are cut at predetermined locations (indicated by dashed lines in Fig. 17) to obtain the semiconductor device E as shown in Fig. 11. The semiconductor device E can be placed into the circuit

substrate in the same state as is the semiconductor device B shown in Fig. 3.

Next, reference is made to Fig. 18 and Fig. 19. These figures show a storage receptacle capable of collectively storing a plurality of the semiconductor devices. Figs. 18 and 19 show the semiconductor devices A according to the first embodiment. However, the storage receptacle can also be used to store the other semiconductor devices such as the conductor device B and the conductor device E.

As shown in Fig. 18, the storage receptacle includes a carrier member H having a plurality of recesses H1, and a cover tape R pasted to the carrier member H to close the recesses H1. The recesses H1 are formed at a predetermined longitudinal interval S. The cover tape R has a adhesive surface R1 to contact the carrier member H and can be peeled off the carrier member H as necessary (See Fig. 19).

As shown in Fig. 18, each semiconductor device A is housed in a corresponding recess H1, with the bottom surface 41 facing upward. In order to accommodate the entire semiconductor device A appropriately while avoiding interference with the light condensing portion 44, each recess H1 includes an upper space H1a having a larger area of section and a lower space H1b having a smaller area of

section. The light condensing portion 44 is housed in the lower space H1b. The carrier member H having the constitution as described above may be formed by embossing an oblong member made of a plastic for example.

For automatically storing a plurality of the semiconductor devices A into the recesses H1, a suction collet operated under a computer control may be used for example. After a predetermined number of the semiconductor devices A are placed appropriately, the cover tape R is pasted to the carrier member H to close each of the recesses. This operation can also be automated.

Each of the semiconductor devices placed in the carrier member H and covered by the cover tape R can be taken out of the storage receptacle in the following steps.

Specifically, referring to Fig. 19, first the cover tape R (See Fig. 18.) pasted to the carrier member H is gradually removed by appropriate means. During this operation, the carrier member H is moved in a direction indicated by Arrow I. On the other hand, the removed cover tape R is moved in a direction indicated by Arrow I' and wound by an unillustrated winding device. This gradually exposes the semiconductor devices A in the recesses H1 of the carrier member H. The exposed semiconductor device

A is sucked by a suction collet K disposed at an appropriate location, and then taken up. In such steps as described above, the semiconductor devices A are taken out of the recesses H, one by one.

According to the method described as above, the semiconductor devices A stored in the storage receptacle can be automatically taken out. Further, after taking out a necessary number of semiconductor devices A, if the remaining cover tape R is left attached to the carrier member H, then the remaining semiconductor devices A can be stored unexposed to the outside air. The carrier member shown in Figs. 18 and 19 is an oblong member. However, the shape of the carrier member H is not limited to this. For example, the recesses H1 for accommodating the semiconductor devices may be provided in a two-dimensional layout in a plate-like container.

CLAIMS

1. (Amended) A semiconductor device comprising:

a semiconductor chip;

a protective package for covering the semiconductor chip, including at least a pair of opposed side surfaces, each of the side surfaces having a first slanted portion and a second slanted portion each being flat and meeting the other at a predetermined angle;

a first lead conducting to the semiconductor chip, including an inner portion covered by the protective package and a plurality of outer portions extending out of the protective package;

a second lead conducting to the semiconductor chip, including an inner portion covered by the protective package and a plurality of outer portions extending out of the protective package;

wherein the inner portions and the outer portions of the first and the second leads are flat, extending in a same plane,

wherein the outer portions of the first lead extend from both of the pair of opposed side surfaces out of the protective package, and

wherein the outer portions of the second lead extend from both of the pair of opposed side surfaces out of the protective package.

2. (Deleted)

3. (Deleted)

4. (Deleted)

5. (Amended) The semiconductor device according to Claim 1, wherein the outer portions of the first and the second leads extend out of the protective package, from places where the first slanted portion and the second slanted portion meet each other.

6. (Amended) The semiconductor device according to Claim 5, wherein the first slanted portion and the second slanted portion meet each other generally at a thickness-wise center of the protective package.

7. The semiconductor device according to Claim 1, wherein the semiconductor chip is a light emitting element.

8. The semiconductor device according to Claim 1, wherein the semiconductor chip is a light receiving element.

9. (Deleted)

10. (Amended) A mounting structure of a semiconductor device on a circuit substrate,

the semiconductor device including: a semiconductor chip; a protective package for covering the semiconductor chip, including at least a pair of opposed side surfaces, each of the side surfaces having a first slanted portion and a second slanted portion each being flat and meeting the other at a predetermined angle; a first lead conducting to the semiconductor chip, including an inner portion covered by the protective package and a plurality of outer portions extending out of the protective package; a second lead conducting to the semiconductor chip, including an inner portion covered by the protective package and a plurality of outer portions extending out of the protective package; the inner portions and the outer portions of the first and the second leads being flat and extending in a same plane; the outer portions of the first lead extending from both of the pair of opposed side surfaces out of the protective package; the outer portions of the second lead extending from both of the opposed side surfaces out of the protective package;

the circuit substrate including: a main surface formed with a predetermined wiring pattern; a plurality of connecting pads formed in the main surface; and a through hole corresponding to a shape of the protective

package;

wherein the protective package is fitted into the through hole and the outer portions of the first lead and the second lead are connected with the connecting pads.

11. The mounting structure according to Claim 10, wherein the connecting pads are disposed around the through hole.

12. The mounting structure according to Claim 10, wherein the main surface mounted with the semiconductor device is laminated with a coating member.

13. (Deleted)

14. (Deleted)

15. (Deleted)

16. (Deleted)

17. (Added) A method for manufacturing a semiconductor device using a lead frame, the lead frame including a pair of side bars and a plurality of pairs of cross bars, each pair of the cross bars including a first cross bar bridging the pair of side bars and having an

intermediate portion formed with a bonding pad and a second cross bar bridging the pair of side bars near the first cross bar, the pair of side bars being interconnected only by the first and the second cross bars; the method comprising:

a semiconductor-chip bonding step of bonding a semiconductor chip to the bonding pad, establishing electrical connection with the first cross bar;

a wire bonding step of electrically connecting the semiconductor chip with the second cross bar located near the first cross bar; and

a protective-package formation step of forming a protective package using a resin, for sealing the semiconductor chip, the wire, part of the first cross bar including the bonding pad, and part of the second cross bar including a portion connected with the wire.

18. (Added) The method according to Claim 17, wherein the lead frame is heated in the wire bonding step.

ABSTRACT

The semiconductor device (A) comprises a semiconductor chip (3), a protective package (4) covering the semiconductor chip (3), a first lead (1), and a second lead (2). The semiconductor chip (3) is placed at an inner end (10a) of the first lead (1). Further, the semiconductor chip (3) is connected to an inner end (20a) of the second lead (2) via a wire (W). The first lead (1) includes an outer portion (11) extending out of the protective package (4) whereas the second lead (2) includes an outer portion (21) extending out of the protective package (4). These two outer portions (11, 21) are flat.

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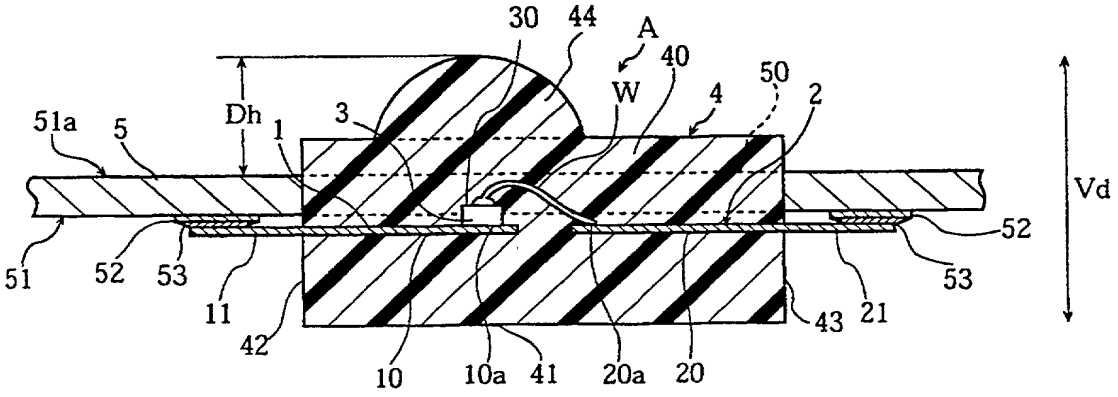
添付公開書類
国際調査報告書

(54)Title: SEMICONDUCTOR DEVICE AND SUBSTRATE FOR SEMICONDUCTOR DEVICE

(54)発明の名称 半導体デバイス及びこれを実装するための基板



(57) Abstract

A semiconductor device (A) comprises a semiconductor chip (3), a protective package (4) covering the semiconductor chip (3), a first lead (1), and a second lead (2). The semiconductor chip (3) is placed on an inner end (10a) of the first lead (1). The semiconductor chip (3) is connected through wire (W) with an inner end (20a) of the second lead (2). The first lead (1) includes an outer part (11) projecting from the protective package (4), and the second lead (2) includes an outer part (21) projecting from the protection package (4). The two outer parts (11, 21) are flat.

FIG.1

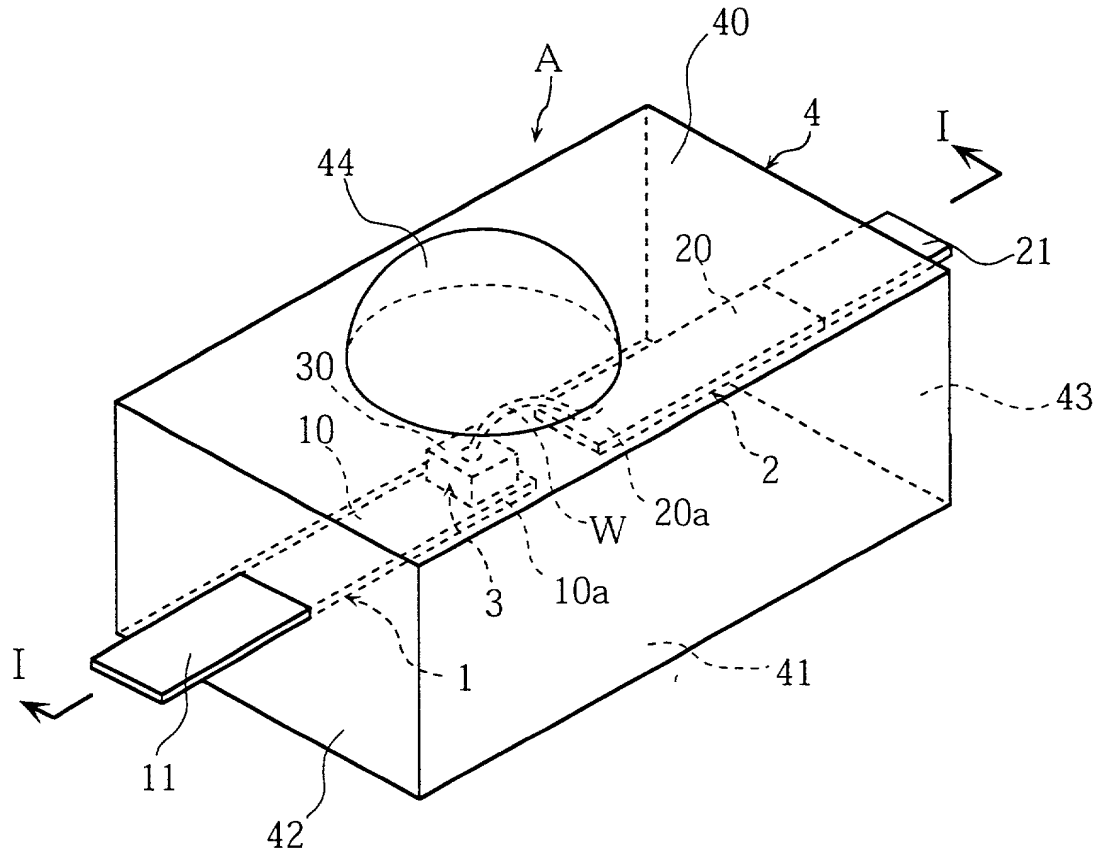


FIG.2

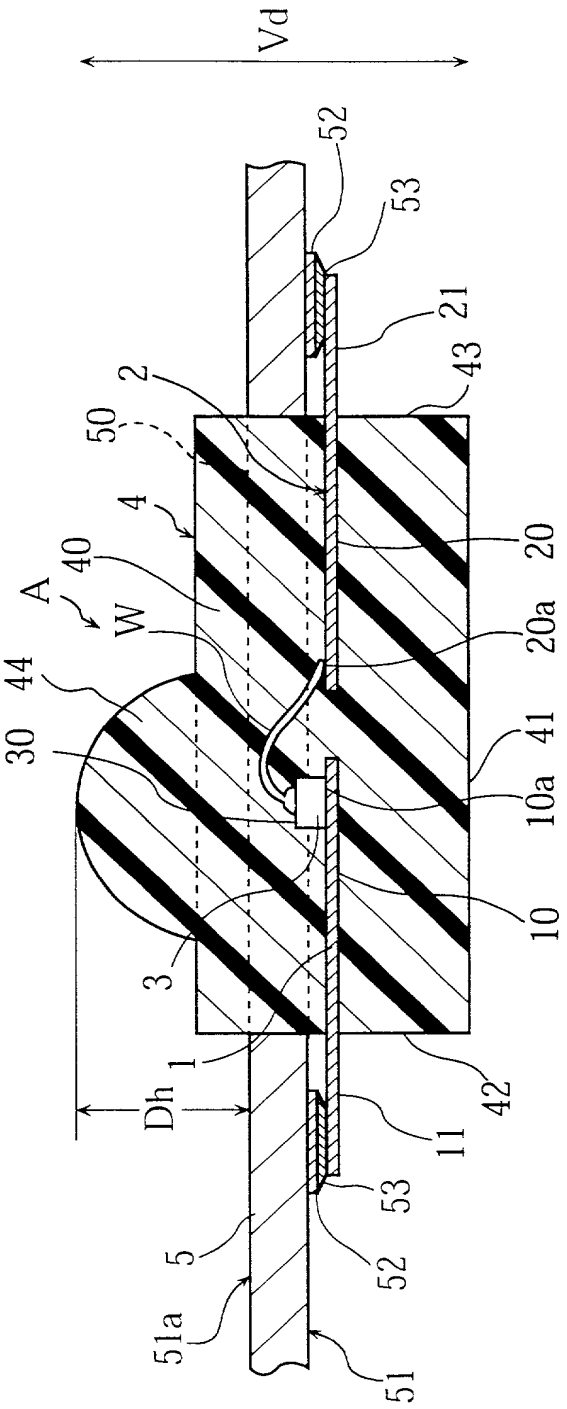

Vd
52
53
21
43
2
50
4
40
A
W
20
20a
44
30
41
10a
10
3
1
Dh
42
11
53
52
5
51a
51

FIG.3

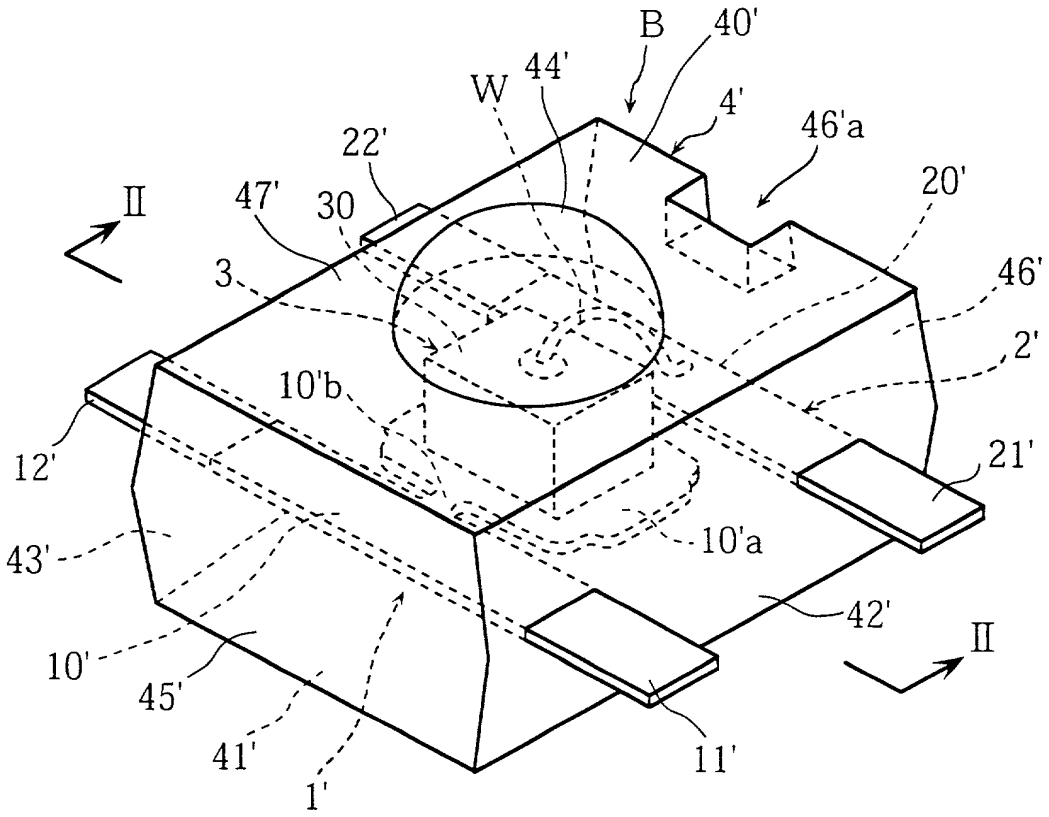


FIG.4

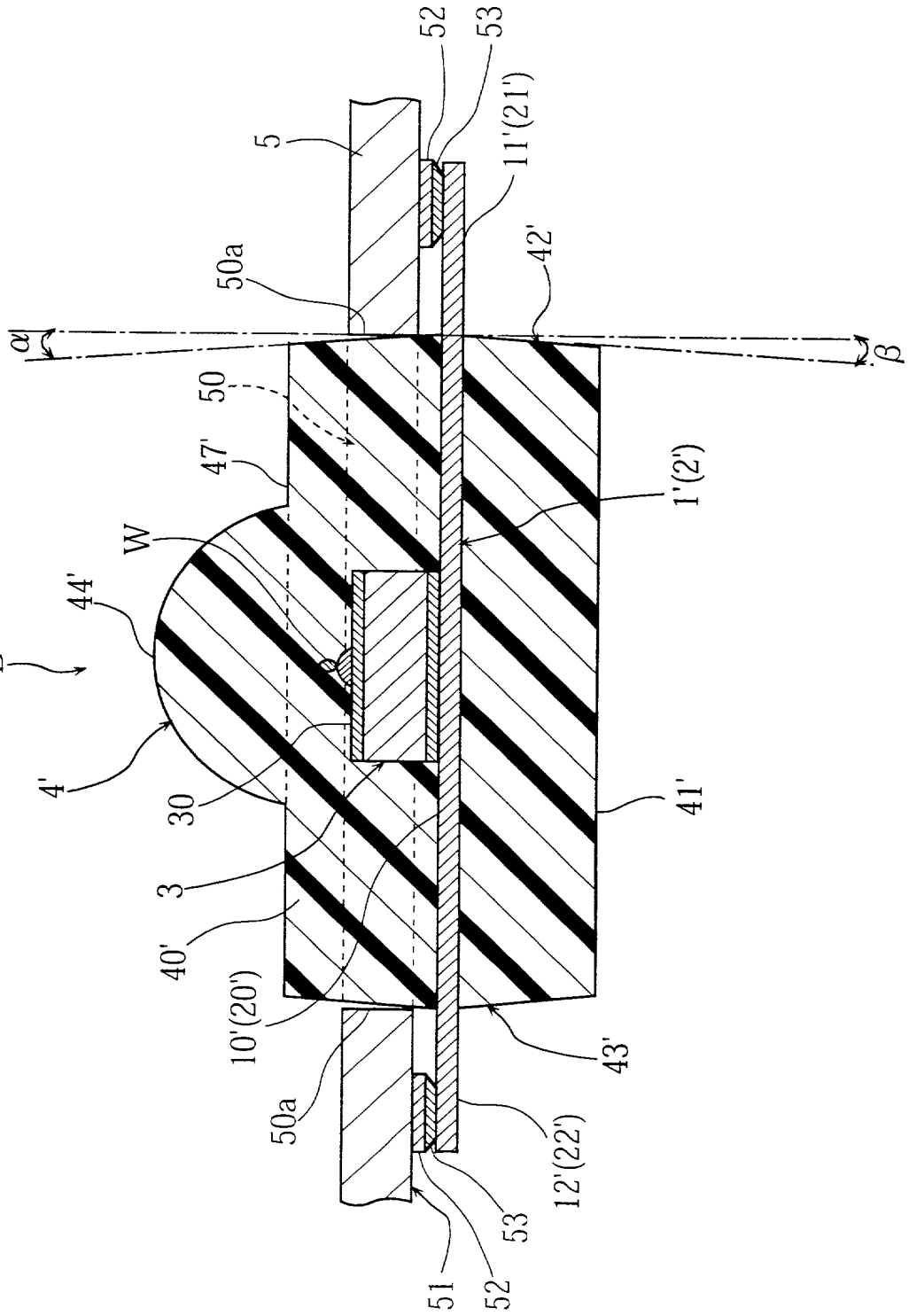

52
53
5
11'(21')
50a
42'
α
β
50
47'
1'(2')
W
44'
B
4'
30
41'
3
40'
10'(20')
43'
50a
12'(22')
53
51
52

FIG.5

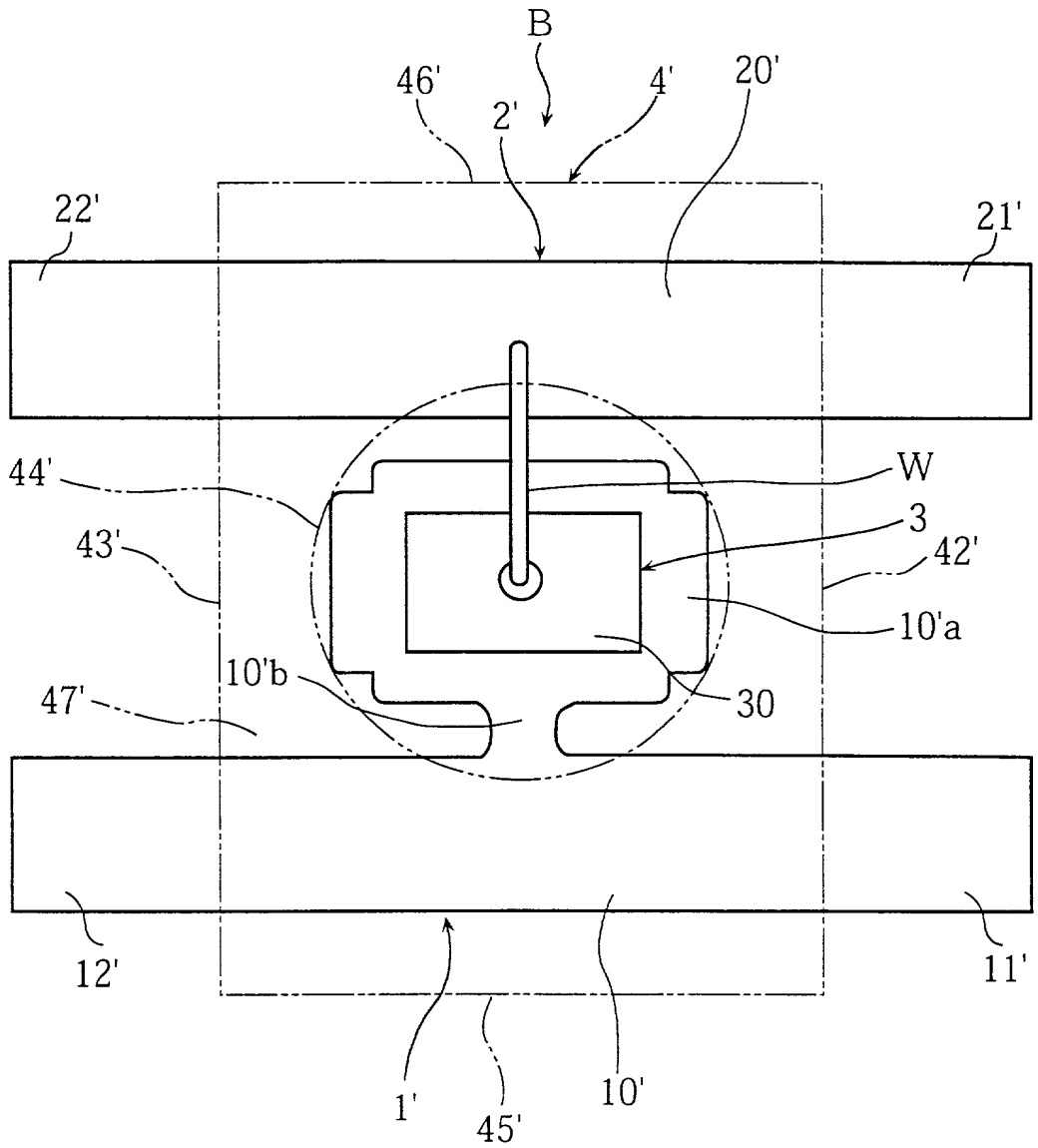


FIG.6

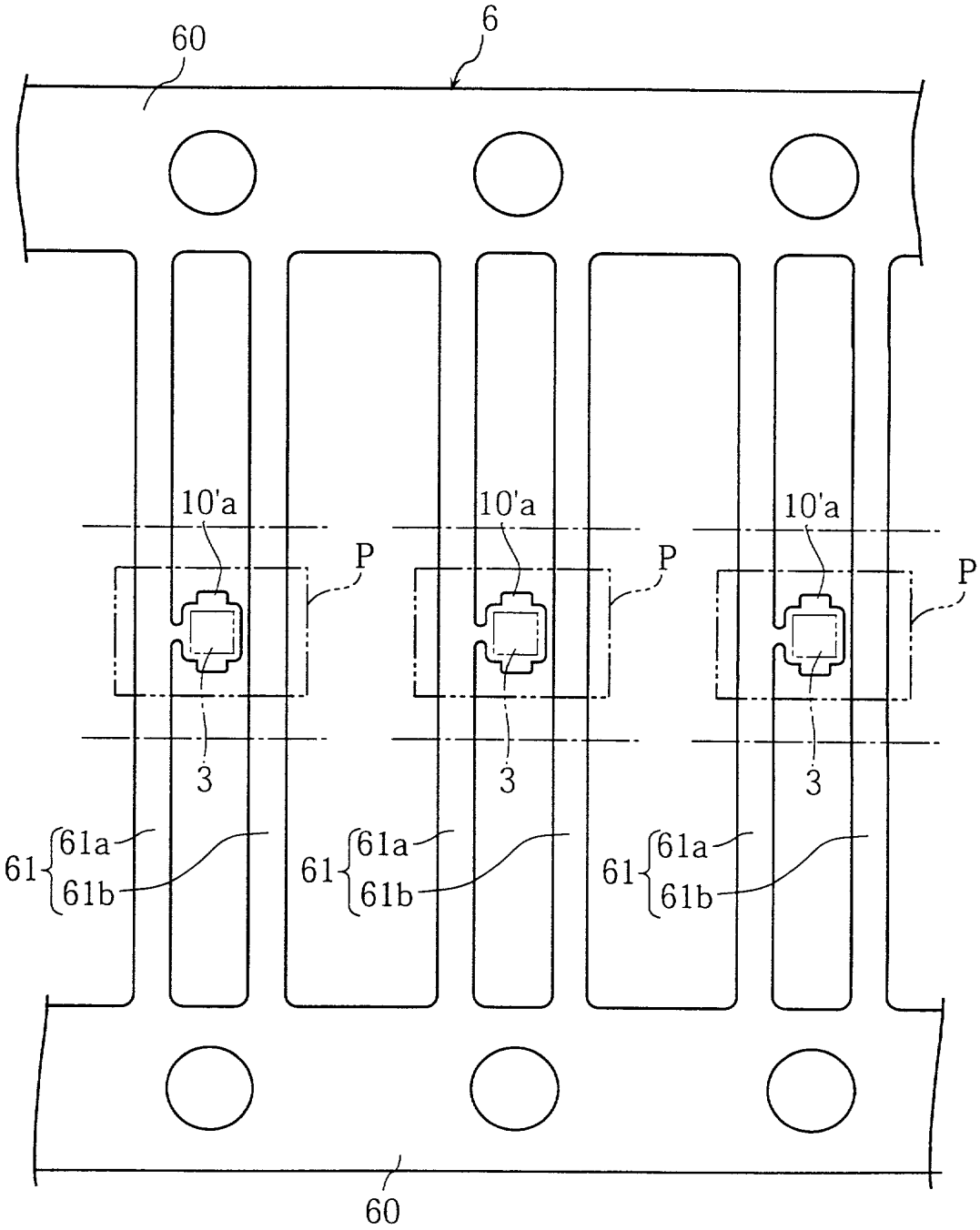


FIG.7

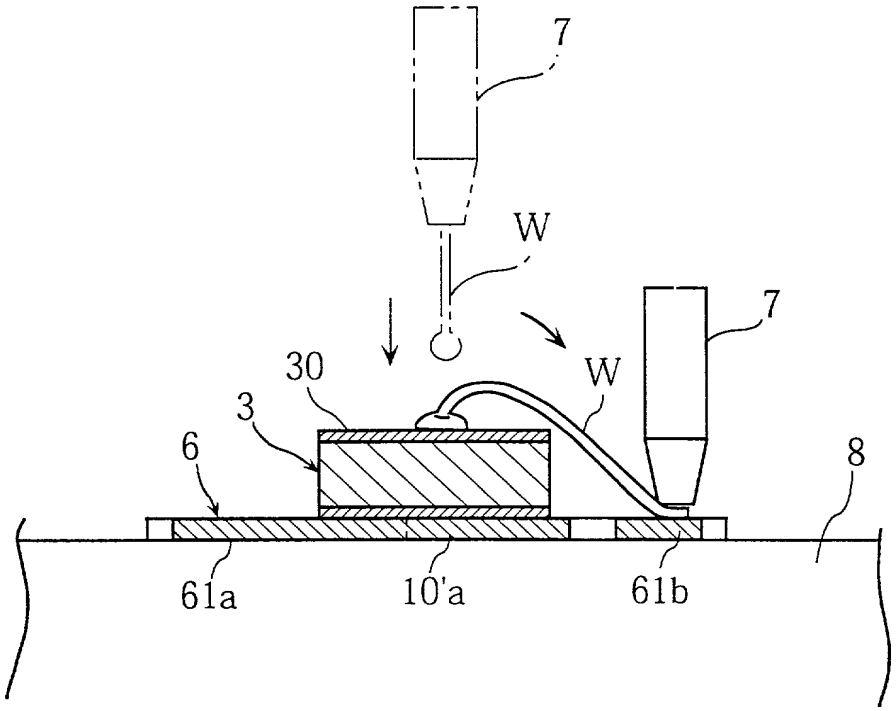


FIG.8

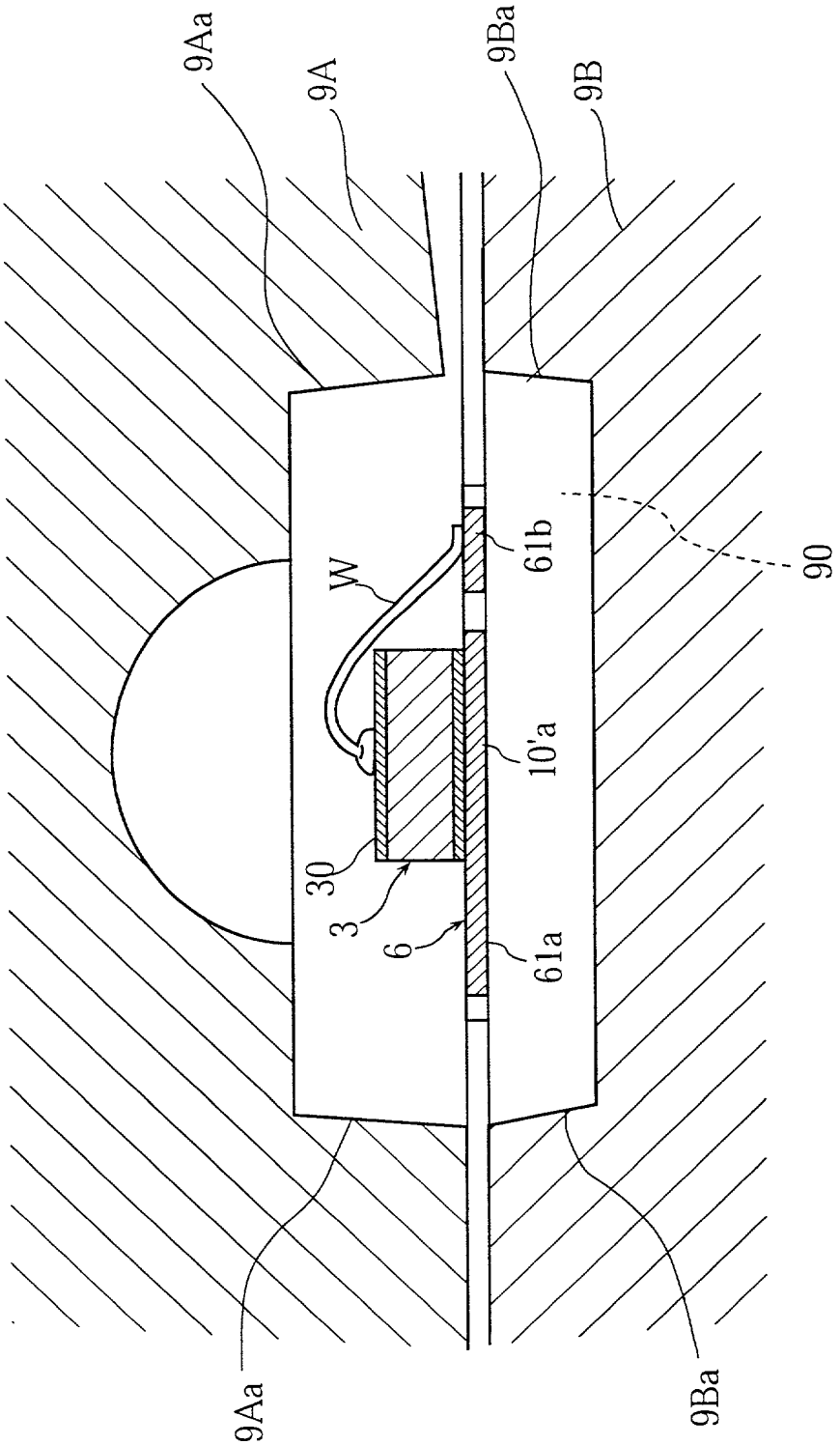


FIG.9

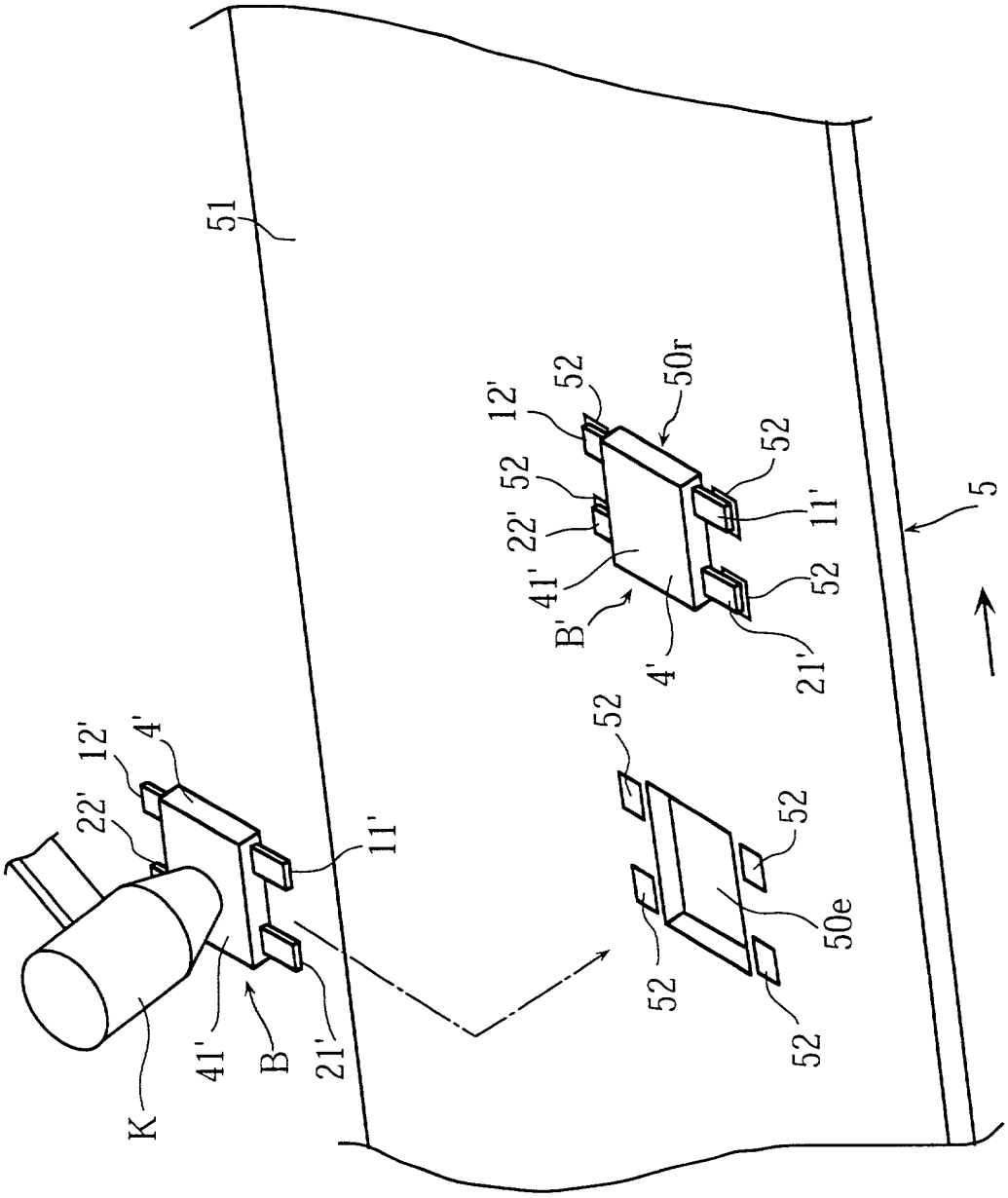


FIG.10

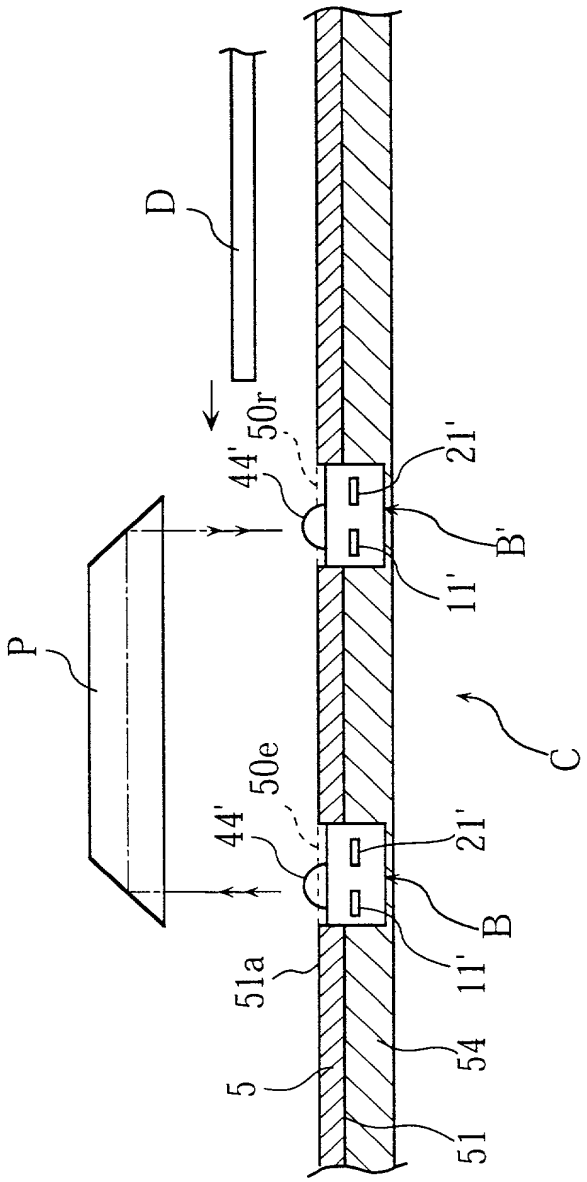


FIG.11

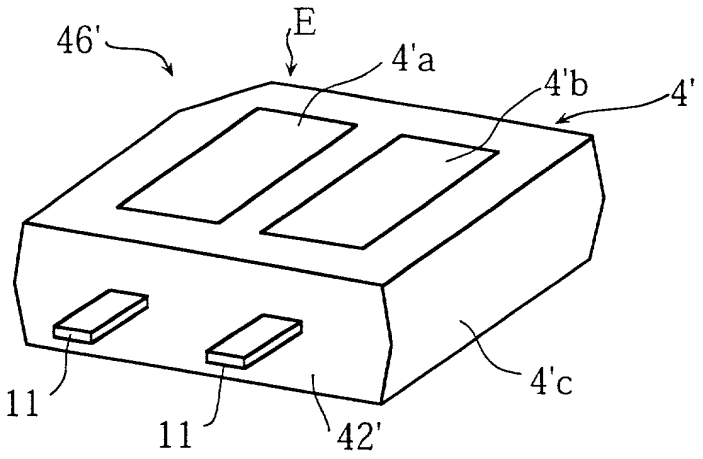


FIG.12

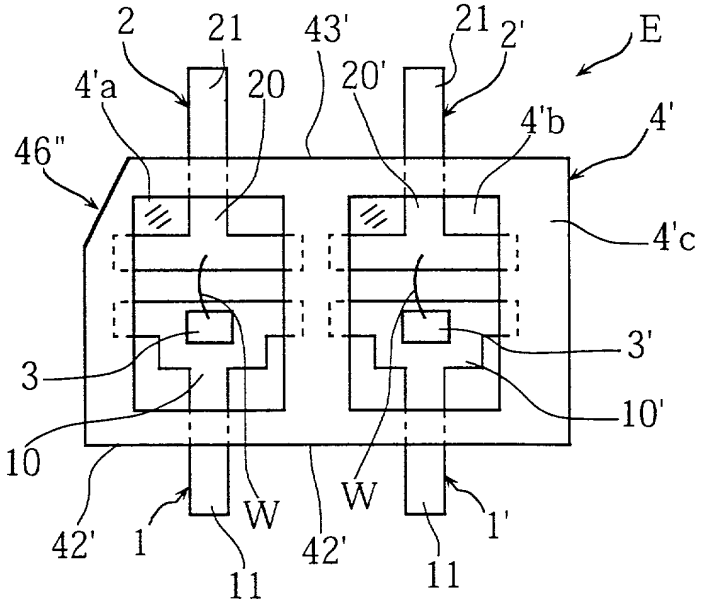


FIG.13

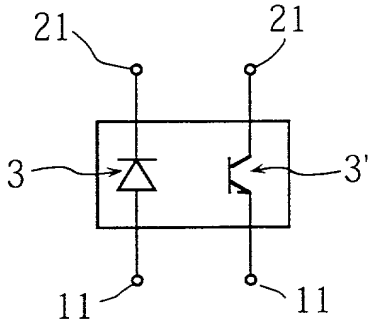


FIG.14

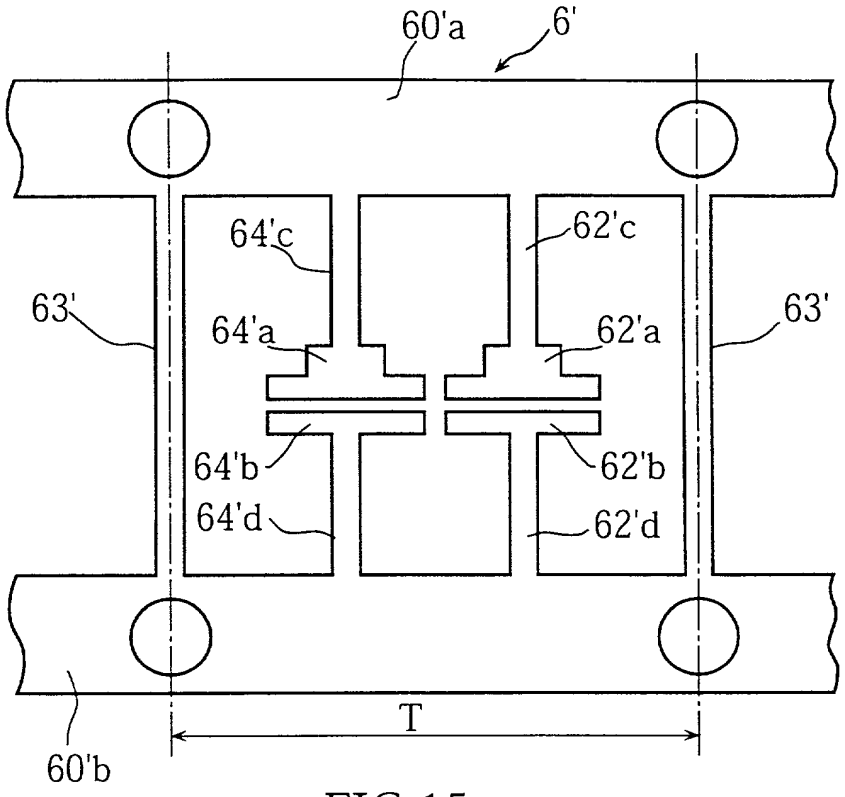

60'a
6'
64'c
62'c
63'
64'a
62'a
63'
64'b
62'b
64'd
62'd
T
60'b

FIG.15

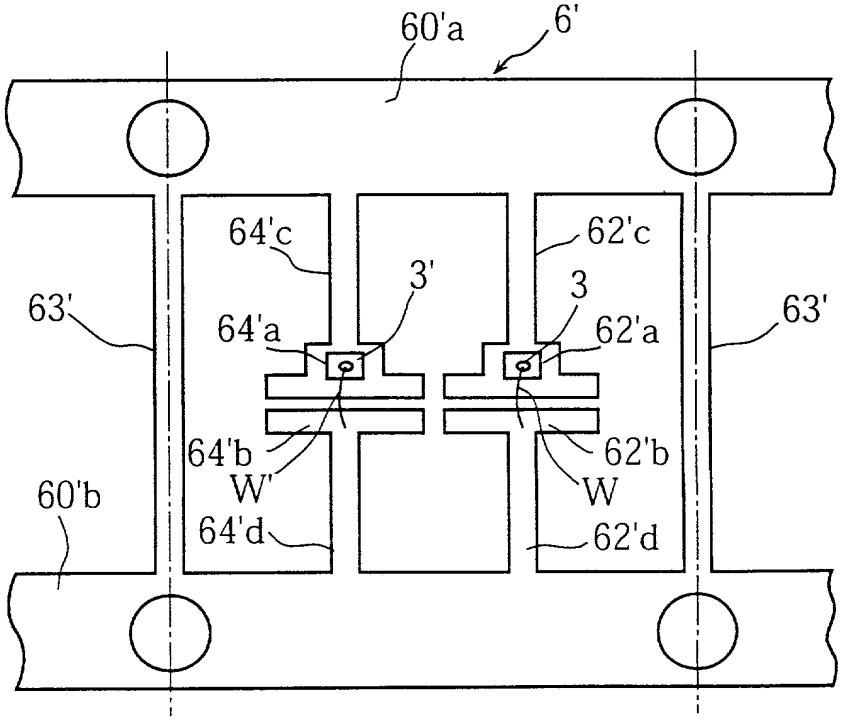

60'a
6'
64'c
62'c
3'
3
63'
64'a
62'a
63'
64'b
62'b
W'
W
60'b
64'd
62'd

FIG.16

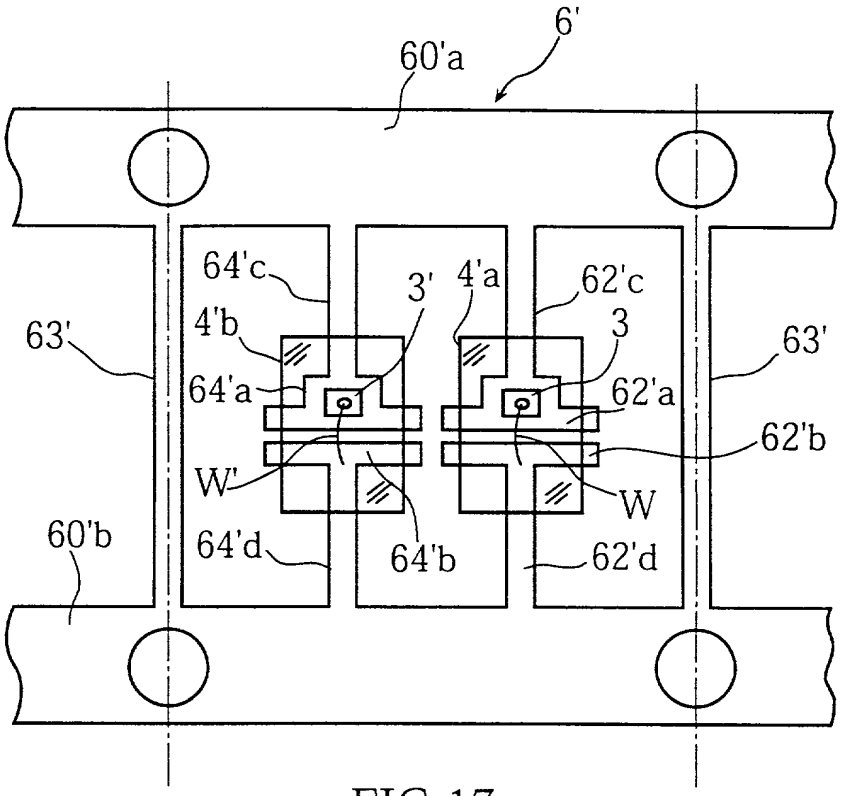

6'
60'a
64'c
3'
4'a
62'c
4'b
3
63'
63'
64'a
62'a
62'b
W'
W
60'b
64'd
64'b
62'd

FIG.17

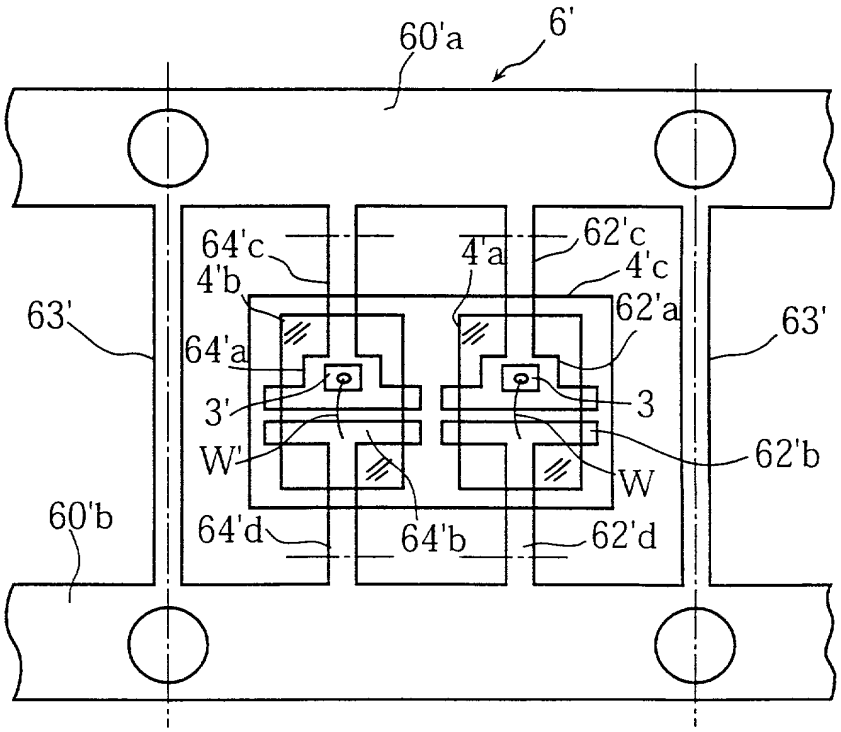

60'a
6'
64'c
4'a
62'c
4'b
4'c
63'
62'a
63'
64'a
3'
3
62'b
W'
W
60'b
64'd
64'b
62'd

FIG.18

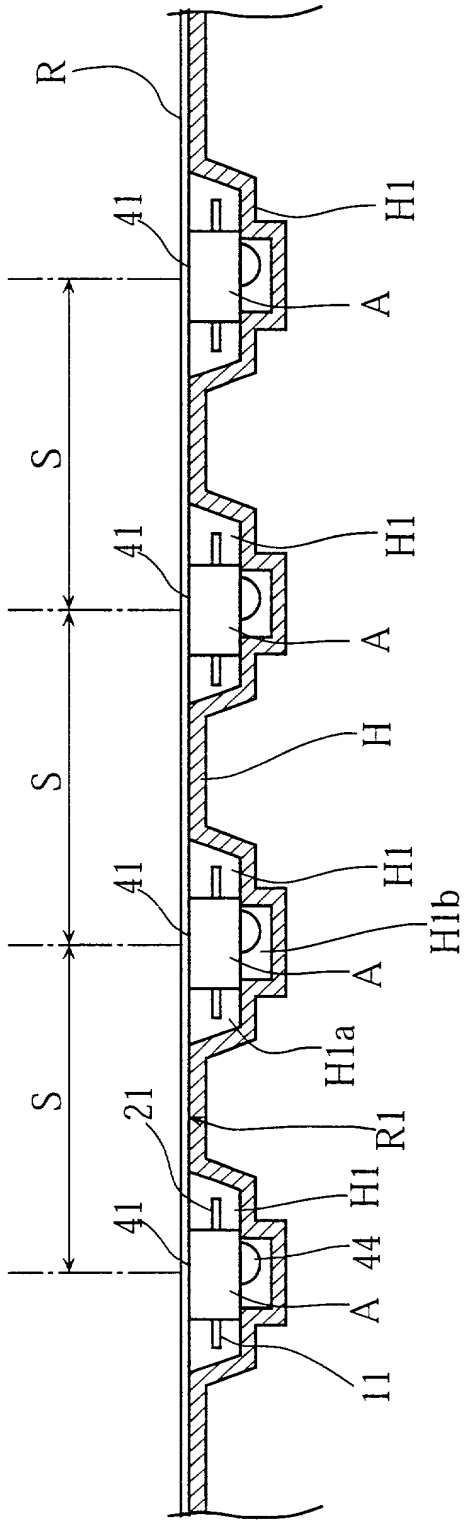


FIG.19

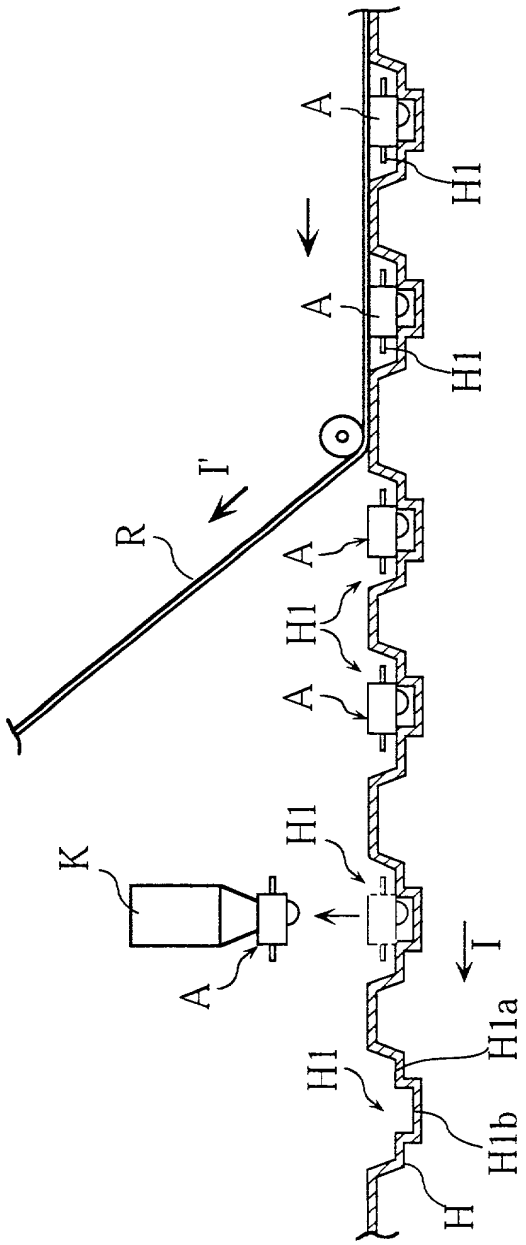


FIG.20

PRIOR ART

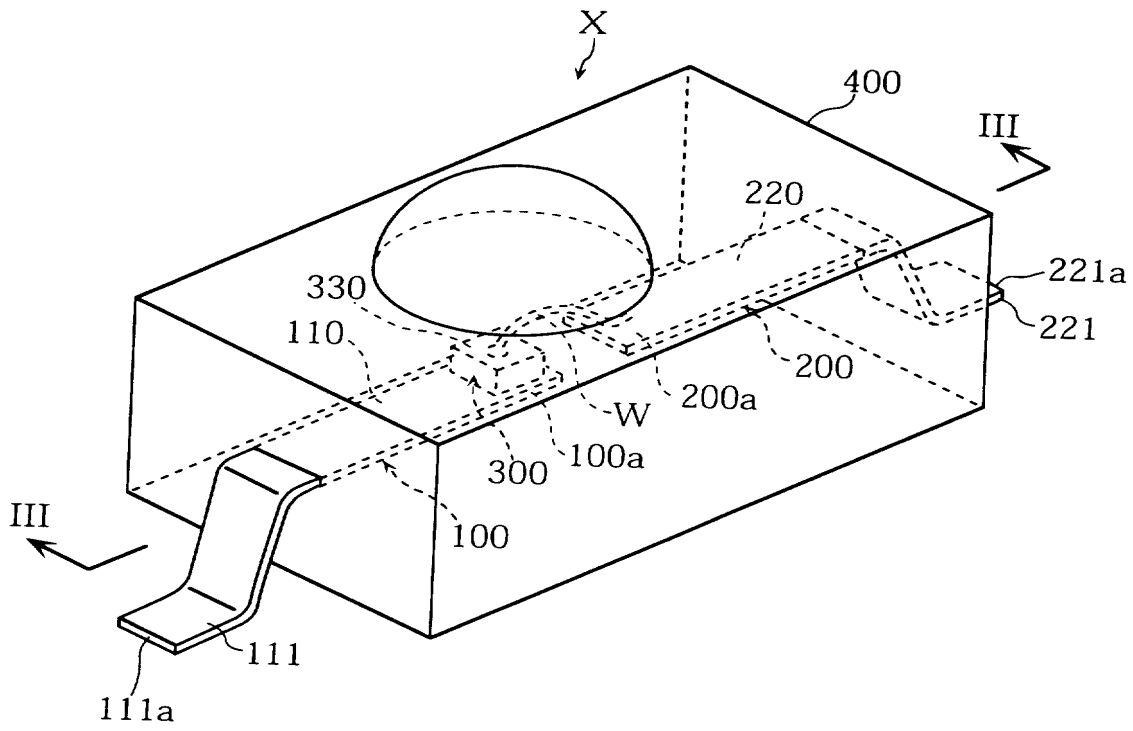
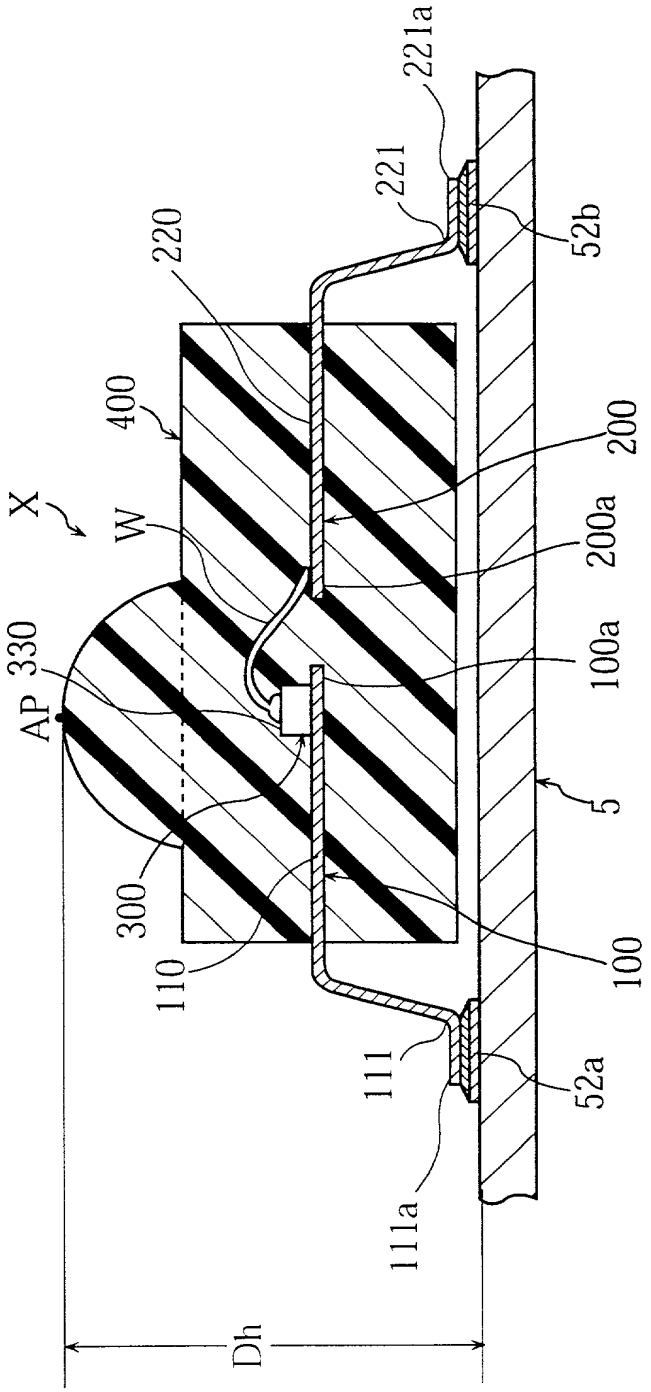


FIG.21
PRIOR ART



Declaration and Power of Attorney For Patent Application
特許出願宣言書

Japanese Language Declaration

私は、下欄に氏名を記載した発明者として、以下のとおり宣言する：

As a below named inventor, I hereby declare that:

私の住所、郵便の宛先および国籍は、下欄に氏名に続いて記載したとおりであり、

My residence, post office address and citizenship are as stated below next to my name,

名称の発明に関し、請求の範囲に記載した特許を求める主題の本来の、最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名が下欄に記載されている場合）と信じ、

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND SUBSTRATE FOR MOUNTING THE SAME

その明細書を
（該当する方に印を付す）

the specification of which
(check one)

☐ここに添付する。

☐is attached hereto.

☐＿＿＿＿＿＿＿＿日に出願番号
第＿＿＿＿＿＿＿＿号として提出し、
＿＿＿＿＿＿＿＿日に補正した。
（該当する場合）

☐was filed on ＿＿＿＿＿＿＿＿ as
Application Serial No.＿＿＿＿＿＿＿＿
and was amended on ＿＿＿＿＿＿＿＿
(if applicable)

☐＿＿＿＿＿＿＿＿日にＰＣＴ国際出願番号
第＿＿＿＿＿＿＿＿号として提出し、
ＰＣＴ第19条に基づき＿＿＿＿＿＿日に補正した。
（該当する場合）

☒was described and claimed in PCT international application No. PCT/JP99/04624 filed on August 26, 1999
and as amended under PCT Article 19 on
＿＿＿＿＿＿＿＿
(if applicable)

私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37部第１章第56条（a）項に従い、本願の審査に所要の情報を開示すべき義務を有することを認める。

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

Japanese Language Declaration

私は、合衆国法典第35部第119条（a）－（d）項または第365条（a）－（b）項にもとづく下記の外国特許出願または発明者証出願または少なくとも１つの合衆国以外の国を指定したＰＣＴ国際出願の外国優先権利益を主張し、さらに優先権の主張に係わる基礎出願の出願日前の出願日を有する外国特許出願または発明者証出願またはＰＣＴ国際出願を以下に明記する：

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Prior foreign applications
先の外国出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願の年月日)	Priority claimed 優先権の主張
Patent Application No. 10-246025	Japan	31/8/1998	☒ Yes あり ☐ No なし
			☐ Yes あり ☐ No なし
			☐ Yes あり ☐ No なし
			☐ Yes あり ☐ No なし
			☐ Yes あり ☐ No なし
			☐ Yes あり ☐ No なし

私は、合衆国法典第35部第120条にもとづく下記の合衆国特許出願の利益または第365条（c）項にもとづく合衆国を指定するＰＣＴ国際出願の利益を主張し、本願の請求の範囲各項に記載の主題が合衆国法典第35部112条第１項に規定の態様で先の合衆国出願に開示されていない限度において、先の出願の出願日と本願の国内出願日またはＰＣＴ国際出願日の間に公表された連邦規則法典第37部第１章第56条（a）項に記載の所要の情報を開示すべき義務を有することを認める：

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (出願番号)	(Filing Date) (出願日)	(現況) (特許済み、係属中、放棄済み) (Status) (patented, pending, abandoned)

Japanese Language Declaration

私は、ここに自己の知識にもとづいて行った陳述がすべて真実であり、自己の有する情報および信ずるところに従って行った陳述が真実であると信じ、さらに故意に虚偽の陳述等を行った場合、合衆国法典第18部第1001条により、罰金もしくは禁固に処せられるか、またはこれらの刑が併科され、またかかる故意による虚偽の陳述が本願ないし本願に対して付与される特許の有効性を損なうことがあることを認識して、以上の陳述を行ったことを宣言する。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

委任状：私は、下記発明者として、以下の代理人をここに選任し、本願の手続を遂行すること並びにこれに関する一切の行為を特許商標庁に対して行うことを委任する。（代理人氏名および登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and /or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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Japanese Language Declaration

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